

IN THE CLAIMS:

Please amend claims 1-4, and add new claims 18-24 as follows:

1. (Currently Amended) A semiconductor integrated circuit on a semiconductor chip, the semiconductor integrated circuit comprising:
 - a single instruction multiple data (SIMD) unit conducting a concurrent operation for a plurality of data items;
 - a data buffer connectible to said SIMD unit; and
 - a data transfer control unit for controlling transfer of data for said data buffer, wherein said data transfer control unit controls the transfer of data for a subsequent operation of the SIMD unit to said data buffer from outside of said semiconductor integrated circuit in concurrence with the current operation of said SIMD unit for ~~the plural~~ a plurality of data items read from said data buffer.
2. (Currently Amended) A semiconductor integrated circuit according to claim 1, wherein said data buffer includes: a dual-port unit including a first port and a second port,
 - said first port being ~~connected~~ coupled via a first bus to said SIMD unit,
 - said second port being ~~connected~~ coupled via a second bus to said data transfer control unit.
3. (Currently Amended) A semiconductor integrated circuit according to claim 2, wherein~~[[:]]~~ said first port ~~concurrently~~ inputs ~~[[and]]~~ or outputs ~~[[the]]~~ said plurality of data items for said first bus~~[[:]]~~, and
 - wherein said second port ~~concurrently~~ inputs ~~[[and]]~~ or outputs ~~[[the]]~~ said plurality of data items for said second bus.
4. (Currently Amended) A semiconductor integrated circuit according to claim 3, wherein said SIMD unit includes:

a first data register ~~connected~~ coupled to said first bus, said first data register being concurrently latched the plurality of data items;

a second data register ~~connected~~ coupled to said first bus, said ~~[[first]]~~ second data register being concurrently latched ~~[[the]]~~ said plurality of data items; and

an operator for receiving ~~[[the]]~~ said plurality of data items respectively latched by said first and second data registers and for conducting a concurrent operation for ~~[[the]]~~ said plurality of data items in said first and second data registers.

5. (Original) A semiconductor integrated circuit according to claim 2, further comprising a central processing unit conducting operation control for said SIMD unit and access control via said first bus to said data buffer.
6. (Withdrawn) A semiconductor integrated circuit, comprising:
 - a single instruction multiple data (SIMD) unit conducting a concurrent operation for a plurality of data items;
 - a data buffer connected via a first bus to said SIMD unit; and
 - a data transfer control unit connected via a second bus to said data buffer,wherein
 - said data transfer control unit includes a bit extension unit for conducting bit extension for each of the plurality of data items transferred via said second bus to said data buffer.
7. (Withdrawn) A semiconductor integrated circuit according to claim 6, wherein said bit extension unit conducts 1-bit code extension according to a lower-most bit of the data.
8. (Withdrawn) A semiconductor integrated circuit according to claim 6, wherein said bit extension unit conducts bit extension for the plurality of data items in a concurrent fashion.

9. (Withdrawn) A semiconductor integrated circuit according to claim 6, further comprising a data aligner in a stage before said bit extension unit for the plurality of data items.
10. (Withdrawn) A semiconductor integrated circuit according to claim 6, wherein said data transfer control unit includes a bit removal unit for removing bits from each of the plurality of data items which are read from said data buffer and which are transferred via said second bus.
11. (Withdrawn) A semiconductor integrated circuit according to claim 10, wherein said bit removal unit removes a higher-most bit from the data.
12. (Withdrawn) A semiconductor integrated circuit according to claim 6, wherein said data buffer includes a dual-port unit including a first port and a second port,
said first port being connected via a first bus to said SIMD unit,
said second port being connected via a second bus to said data transfer control unit.
13. (Withdrawn) A semiconductor integrated circuit according to claim 12, wherein:
said first port concurrently input and output the plurality of data items for said first bus; and
said second port concurrently input and output the plurality of data items for said second bus.
14. (Withdrawn) A semiconductor integrated circuit according to claim 13, wherein said SIMD unit comprises:
a first data register connected to said first bus, said first data register being concurrently latched the plurality of data items;

a second data register connected to said first bus, said first data register being concurrently latched the plurality of data items; and

an operator for receiving the plurality of data items respectively latched by said first and second data registers and for conducting a concurrent operation for the data items.

15. (Withdrawn) A semiconductor integrated circuit according to claim 14, further comprising a central processing unit conducting operation control for said SIMD unit and access control via said first bus to said data buffer.
16. (Withdrawn) A semiconductor integrated circuit according to claim 15, wherein
said first and second data registers latch, in compression processing of image data, the image data;
said first data register latches, in expansion of image data, the image data; and
said second data register latches data of inverse discrete cosine transform (IDCT).
17. (Withdrawn) A semiconductor integrated circuit, comprising:
a single instruction multiple data (SIMD) unit conducting a concurrent operation for a plurality of data items;
a data buffer connectible to said SIMD unit;
a data transfer control unit for controlling transfer of data for said data buffer;
and
a bit extension unit disposed on a data transfer path connecting said data buffer to said SIMD unit for conducting bit extension for each of the plurality of data items to said SIMD unit in a concurrent fashion.
18. (New) A semiconductor integrated circuit according to claim 1, wherein said data transfer control unit includes a bit extension unit for conducting bit extension for each

of said plurality of data items transferred via said second bus to said data buffer.

19. (New) A semiconductor integrated circuit according to claim 18, wherein said bit extension unit conducts 1-bit code extension according to a lower-most bit of said plurality of data items.
20. (New) A semiconductor integrated circuit according to claim 18, wherein said bit extension unit conducts bit extension for said plurality of data items in a concurrent fashion.
21. (New) A semiconductor integrated circuit according to claim 18, further comprising a data aligner in a stage before said bit extension unit for said plurality of data items.
22. (New) A semiconductor integrated circuit according to claim 18, wherein said data transfer control unit includes a bit removal unit for removing bits from each of said plurality of data items which are read from said data buffer and which are transferred via said second bus.
23. (New) A semiconductor integrated circuit according to claim 22, wherein said bit removal unit removes a higher-most bit from said plurality of data items.
24. (New) A semiconductor integrated circuit according to claim 4, wherein said first and second data registers latch image data when being in compression processing of image data, and
wherein said first data register latches image data and said second data register latches data of inverse discrete cosine transform (IDCT) when being in expansion of image data.